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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,865	01/07/2005	Hendrik Hubertus Van Der Meer	NL02 0677 US	4438

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/520,865	VAN DER MEER ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 8, 9, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Gilbert et al. (U.S. 5,744,841).

Regarding claim 1, Gilbert et al. teaches a method of forming on a semiconductor substrate (**30** in Fig. 3) an electrostatic discharge protecting device together with internal circuitry to be protected by said protecting device, said method comprising the steps of:

a) forming an offset transistor arrangement in said protecting device (**22** in Fig. 3); and

b) increasing an acceptor concentration at said offset transistor arrangement so as to selectively reduce a breakdown voltage of said offset transistor arrangement (boron implant **32** in Fig. 3; column 2, lines 47-67).

Regarding claim 2, Gilbert et al. teaches the method according to claim 1, wherein said offset transistor arrangement comprises an offset gate NMOS transistor (column 2, lines 58-62).

Regarding claim 3, Gilbert et al. teaches the method according to claim 1, further comprising the step of using a blanket ion implantation to increase said acceptor concentration (column 3, lines 1-4 disclose performing the implantation without a mask).

Regarding claim 8, Gilbert et al. teaches a method according to claim 1, further comprising the step of using an additional ESD photomask and subsequent ion implantation to increase said acceptor concentration at said offset transistor arrangement (column 3, lines 4-9).

Regarding claim 9, Gilbert et al. teaches a method according to claim 8, wherein said additional ESD photomask and subsequent ion implantation are adapted to obtain a clamping effect based on avalanche breakdown (column 4, lines 13-30).

Regarding claim 11, Gilbert et al. teaches an integrated circuit arrangement comprising an electrostatic discharge protecting device and internal circuitry to be protected by said protecting device, wherein said protecting device comprises an offset transistor arrangement having a locally increased acceptor concentration so as to selectively reduce a breakdown voltage of said offset transistor arrangement (Figs. 3-5—internal circuitry not illustrated, but is inherently present, since the purpose of the ESD protection device is to protect the internal circuitry; column 2, lines 47-67; column 3, lines 27-52).

Claims 1, 2, 7, 8, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu et al. (U.S. 6,040,222).

Regarding claim 1, Hsu et al. teaches a method of forming on a semiconductor substrate (**50** in Fig. 2) an electrostatic discharge protecting device (**56** in Fig. 2) together with internal circuitry (**54** in Fig. 2) to be protected by said protecting device, said method comprising the steps of:

a) forming an offset transistor arrangement in said protecting device (**60** in Fig. 3); and

b) increasing an acceptor concentration at said offset transistor arrangement so as to selectively reduce a breakdown voltage of said offset transistor arrangement (Fig. 2D; paragraph bridging columns 3 and 4).

Regarding claim 2, Hsu et al. teaches the method according to claim 1, wherein said offset transistor arrangement comprises an offset gate NMOS transistor (column 3, lines 65-66).

Regarding claim 7, Hsu et al. teaches the method according to claim 1, further comprising the step of using a p-LDD photomask modified such that it allows to increase said acceptor concentration at said offset transistor arrangement (photoresist layer **82** in Figs. 2C-2D; column 3, lines 53-61).

Regarding claim 8, Hsu et al. teaches a method according to claim 1, further comprising the step of using an additional ESD photomask and subsequent ion implantation to increase said acceptor concentration at said offset transistor arrangement (photoresist layer **82** in Figs. 2C-2D; column 3, lines 53-61).

Regarding claim 11, Hsu et al. teaches an integrated circuit arrangement comprising an electrostatic discharge protecting device (**56** in Fig. 2) and internal circuitry (**54** in Fig. 2) to be protected by said protecting device, wherein said protecting device comprises an offset transistor arrangement (**60** in Fig. 2A) having a locally increased acceptor concentration so as to selectively reduce a breakdown voltage of said offset transistor arrangement (P+ regions in Fig. 2D).

Claims 1-6, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu (U.S. 5, 897,.348).

Regarding claims 1-4, Wu teaches a method of forming on a semiconductor substrate an electrostatic discharge protecting device together with internal circuitry to be protected by said protecting device, said method comprising the steps of:

a) forming an offset gate NMOS transistor—further limited by claim 2—arrangement in said protecting device (**102** in Figs. 1-10); and

b) increasing an acceptor concentration at said offset transistor arrangement so as to selectively reduce a breakdown voltage of said offset transistor arrangement (blanket ion implantation—further limited by claim 3—indicated by arrows in Fig. 1 cause p LDD regions **106**—further limited by claim 4; column 3, lines 55-61).

Regarding claims 5 and 6, Wu teaches the method according to claim 1, further comprising the step of performing photolithography and a subsequent n-LDD—further limited by claim 6—donor ion implantation at said internal circuitry using a dose sufficient to compensate the later-performed blanket acceptor ion implantation in regular NMOS transistors (Fig 3; column 4, lines 4-14; column 5, lines 57-64).

Regarding claim 10, Wu teaches the method according to claim 1, further comprising the step of performing an additional blanket acceptor ion ESD implantation after formation of an n-LDD structure, wherein an n-LDD ion implantation dose should be high enough to compensate the blanket ESD ion implantation in regular NMOS transistors (column 3, line 49 – column 4, line 14; column 5, lines 57-64).

Regarding claim 11, Wu teaches an integrated circuit arrangement comprising an electrostatic discharge protecting device and internal circuitry to be protected by said protecting device, wherein said protecting device comprises an offset transistor arrangement having a locally increased acceptor concentration so as to selectively reduce a breakdown voltage of said offset transistor arrangement (column 3, lines 49-63).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

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